

ABSTRACT

A plurality of connection holes 24 for connecting n^+ type semiconductor region 20 of zener diodes (D_1 , D_2) and wires 21 and 22 to each other are not arranged in the center of the n^+ type semiconductor region 20, that is, in a region in which a p^+ type semiconductor region 6 and the n^+ type semiconductor region 20 form a junction but is arranged in the periphery which is deeper than the center in junction depth. In addition, these connection holes 24 are spaced from each other so that a pitch between the adjacent connection holes 24 is greater than a minimum pitch between connection holes of the circuit, and thereby a substrate shaving quantity is reduced when the respective connection holes 24 are formed by means of dry etching.

(Selected Figure: FIG. 4)